REMARKS

Claims 1-21 were remain pending in the application. Claims 1 and 12 have been amended. Claims 22-29 have been added. Accordingly, Claims 1-29 are now pending in the application.

Support for claims 22 may be found, for example, on page 41, line 18, page 5 lines 11-14, page 2 lines 9-13, page 20 lines 1-9, page 13, lines 22-25, and page 19 lines 1-12 of Applicant's Specification. Support for claim 23 may be found, for example, on page 38 lines 11-13. Support for claim 24 may be found, for example, on page 39 lines 11-18. Support for claim 25 may be found, for example, on page 39 lines 20-28. Support for claim 26 may be found, for example, on page 40 lines 12-15. Support for claim 27 may be found, for example, on page 38 lines 25-28. Support for claim 28 may be found, for example, on page 41 lines 2-3, and page 42, lines 10-27. Support for claim 29 may be found, for example, on page 40 line 22 – page 42 line 8, page 38 lines 3-5, and page 28 line 12 – page 33 line 23.

Specification

In the Office Action, the Examiner requested the status of related applications. Accordingly, the UK patent (GB 2369692, filed November 29, 2000) corresponding to this US application was granted October 16, 2002.

35 U.S.C § 112 Rejections

Claims 1-21 were rejected under 35 U.S.C § 112, first paragraph, as failing to comply with the written description requirement. The Examiner contends that the "added new limitation "operable to respond to a fault state by controlling the copying of the dirtied blocks of the main memory" was not described in the specification at the time the application was filed, had possession of the claimed invention." Applicant respectfully submits that the amendment to claims 1 and 12 overcomes this rejection. Support for

claims 1 and 12 may be found, for example, on page 2 lines 9-13, page 3 lines 9-10, page 4 lines 10-17, page 5 lines 11-14, page 13 lines 22-25, page 19 lines 1-12, page 20 lines 1-5, page 37 lines 20-27, page 38 lines 1-4 and 12, page 39 line 26, page 40 lines 1-10, and page 41 line 18 ("reintegration following an error state") of Applicant's Specification.

35 U.S.C § 102 Rejections

Claims 1-21 were rejected under 35 U.S.C. § 102(a) as being anticipated by Rowlinson et al. (WO 99/66402) or 35 U.S.C. § 102(b) as being anticipated by Garnett (USPN 5,991,900). Applicant respectfully traverses this rejection.

Claim 1 recites, in pertinent part, "the bridge includes **a direct memory access controller** that is operable to respond to an error state by controlling the copying of the dirtied blocks of the main memory of the first processing set indicated in the dirty memory of the first processing set to the main memory of another processing set". The Examiner contends that Rowlinson teaches the highlighted features of claim 1 on page 20 (bottom), page 24 lines 5-10, and page 23 (middle), and that Garnett teaches the highlighted features of claim 1 at column 19 lines 37-50 and column 23 lines 9-16. Applicant strongly disagrees with the Examiner's assertion.

While Rowlinson teaches, on page 20 lines 40-47 (and also on page 20 line 48 – page 22 line 28), and Garnett teaches, at column 19 lines 37-50 (and also at column 19 line 51 – column 21 line 52), that a device may perform direct memory accesses via the bridge 12, Rowlinson and Garnett fail to teach or suggest the features of claim 1 highlighted above. Also, while Rowlinson teaches, on page 23 lines 17-18, and Garnett teaches, at column 22 lines 35-38, that DMA writes may change (or dirty) pages of memory during the time period that the primary processing set is copying the originally dirtied pages of memory from the primary processing set to the other processing set (i.e., copy pass), Rowlinson and Garnett fail to teach or suggest the features of claim 1 highlighted above.

Additionally, page 24 lines 5-16 of Rowlinson and column 23 lines 4-29 of Garnett fail to teach or suggest the features of claim 1 highlighted above. In fact, these sections teach away from the features of claim 1 highlighted above in that they teach "If more than the predetermined number of bits have been set, then **the processor** in stage S45 **copies those pages of its memory 56 which have been dirtied**, as indicated by the dirty bits read from the dirty RAM 124 in stage S43, **to the memory 56 of the other processing set**. Control then passes back to stage S43" and "If, in stage S44, it is determined less than the predetermined number of bits have been written in the dirty RAM 124, then in Stage S45 the primary processor causes the bridge to inhibit DMA requests...thereby denying access of the DMA devices...During the period in which DMA accesses are prevented, the **primary processor** then makes a final **copy pass from its memory to the memory 56 of the other processor** for those memory pages corresponding to the bits set in the dirty RAM 124". (Emphasis added)

Furthermore, Rowlinson teaches, on page 22 line 29 – page 23 line 6, and Garnett teaches, at column 21 line 53 – column 22 line 17,

> "There now follows a description of an example of a mechanism for enabling automatic recovery from an EState (see Figure 11)."
>
> "The automatic recovery process includes reintegration of the state of the processing sets to a common status in order to attempt a restart in lockstep. To achieve this, **the processing set** which asserts itself as the primary processing set as described above copies its complete state to the other processing set. This involves ensuring that the content of the memory of both processors is the same before trying a restart in lockstep mode."
>
> "However, a **problem with the copying of the content of the memory from one processing set to the other** is that **during this copying process a device** connected to the D bus 22 **might attempt to make a direct memory access** (DMA) request for access to the memory of the primary processing set. If DMA is enabled, then a write made to an area of memory which has already been copied would result in the memory state of the two processors at the end of the copy not being the same. In principle, it would be possible to inhibit DMA for the whole of the copy process. However, this would be undesirable, bearing in mind that it is desirable to MINIMISE the time that the system or the resources of the system are unavailable. As an alternative, it would be possible to retry the whole

copy operation when a DMA operation has occurred during the period of the copy. However, it is likely that further DMA operations would be performed during the copy retry, and accordingly this is not a good option either. Accordingly, in the present system, a dirty RAM 124 is provided in the bridge. As described earlier the dirty RAM 124 is configured as part of the bridge SRAM memory 126." (Emphasis added)

Accordingly, while Rowlinson and Garnett teach that DMA writes may be performed which may dirty pages of memory, and teach that a primary processing set copies its complete state to the other processing set to attempt to restart a lockstep, Rowlinson and Garnett fail to teach or suggest "the bridge includes **a direct memory access controller** that is operable to respond to an error state by controlling the copying of the dirtied blocks of the main memory of the first processing set indicated in the dirty memory of the first processing set to the main memory of another processing set" as recited in claim 1.

In accordance, claim 1 is believed to patentably distinguish over Rowlinson and Garnett. Claims 2-11 depend on independent claim 1 and are therefore believed to patentably distinguish over Rowlinson and Garnett for at least the reasons given above.

Furthermore, independent claim 12 recites features similar to those highlighted above with respect to independent claim 1, specifically "**a direct memory access controller** in the bridge responding to an error state by controlling the copying of dirtied blocks of the main memory of the first processing set indicated in the dirty memory of the first processing set to the main memory of another processing set". Claim 12 is therefore believed to patentably distinguish over Garnett and Rowlinson for at least the reasons given in the above paragraphs discussing claim 1. Claims 13-21 depend on independent claim 12 and are therefore believed to patentably distinguish over Rowlinson and Garnett for at least the same reasons.

In addition, after considering the arguments presented below, Applicant respectfully requests the Examiner to show support for the Examiner's assertion that claims 2 and 9 are unpatentable over Garnett.

With regard to claims 2 and 9, the Examiner contends that Garnett discloses the features of claims 2 and 9 at col. 22 line18 - col. 23 line 29. The Applicant finds no evidence to support this statement in the cited location. To the contrary, at column 23, lines 1 and 2, Garnett teaches the primary processing set (**not "the direct memory access controller"** as recited in claims 2 and 9) reads the dirty RAM 124". For at least this additional reason, claims 2 and 9 are believed to patentably distinguish over Garnett. Claims 13 and 20 recites features that are similar to those recited in claims 2 and 9, respectively, and are therefore believed to patentably distinguish over Garnett for at least the same reason.

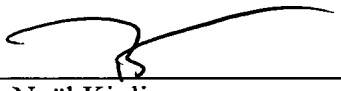
Also, Applicant respectfully requests examination of added Claims 22-29, which are believed to patentably distinguish over the cited references, whether alone or combined.

CONCLUSION

In light of the foregoing amendments and remarks, Applicant submits that all pending claims are now in condition for allowance, and an early notice to that effect is earnestly solicited. If a phone interview would speed allowance of any pending claims, such is requested at the Examiner's convenience.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-02700/BNK.

Respectfully submitted,



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